An 8-bit 8-stage FIR Filter using the CMOS 28nm FDSOI Technology

Implementation and Simulation of TSPC Flipflop, CLA Adder and 8-bit radix-4 Booth Multiplier

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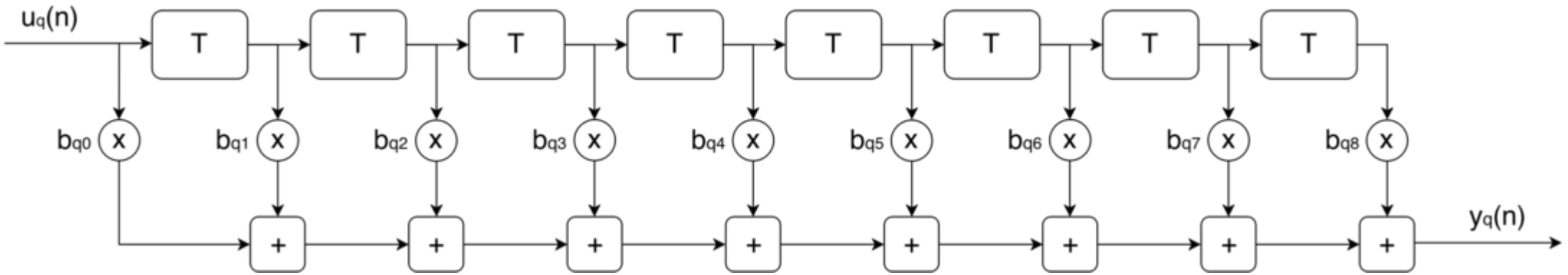
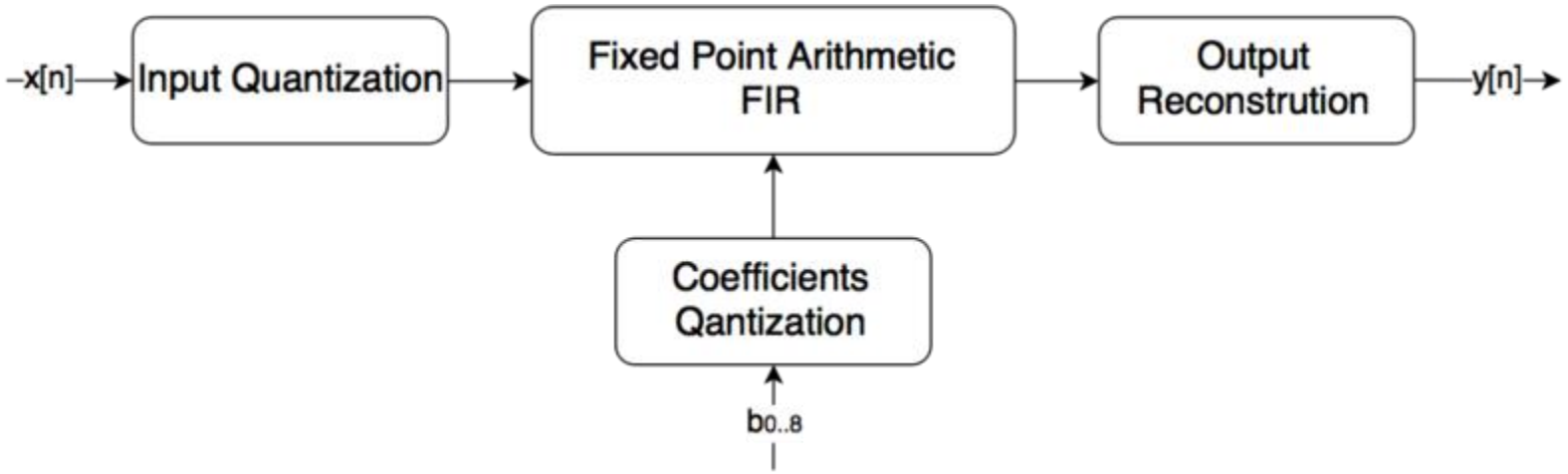
FIR overview

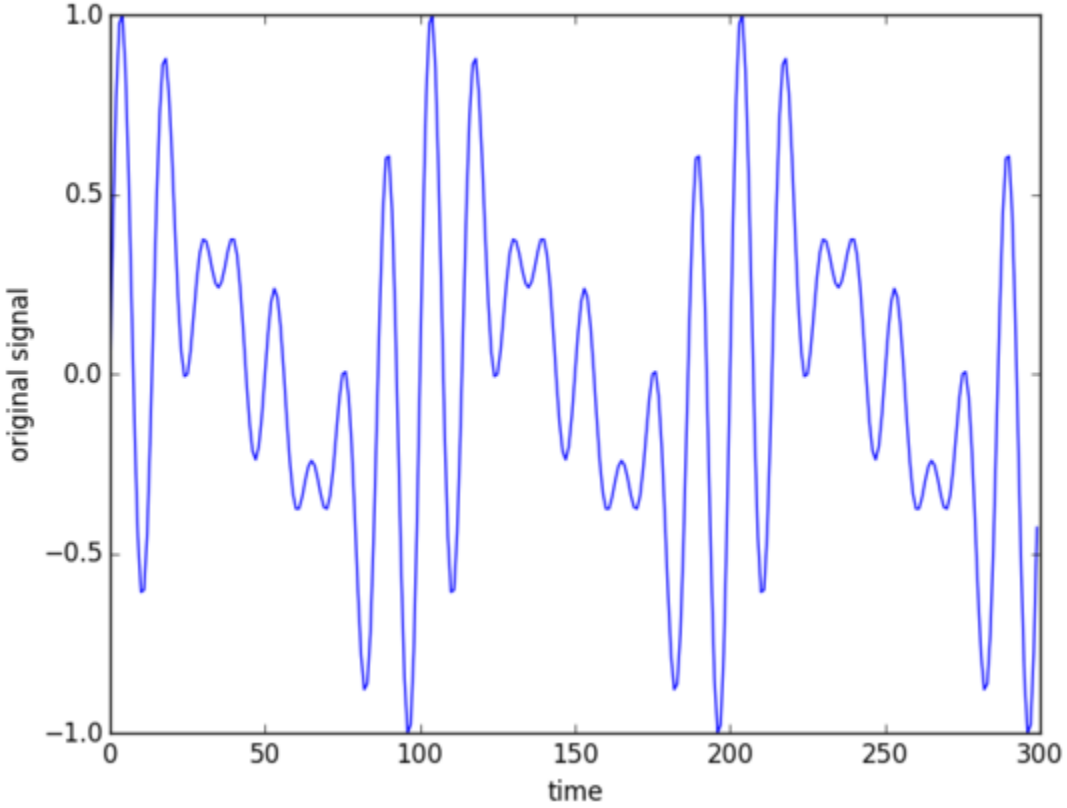


Simulation as proof of concept

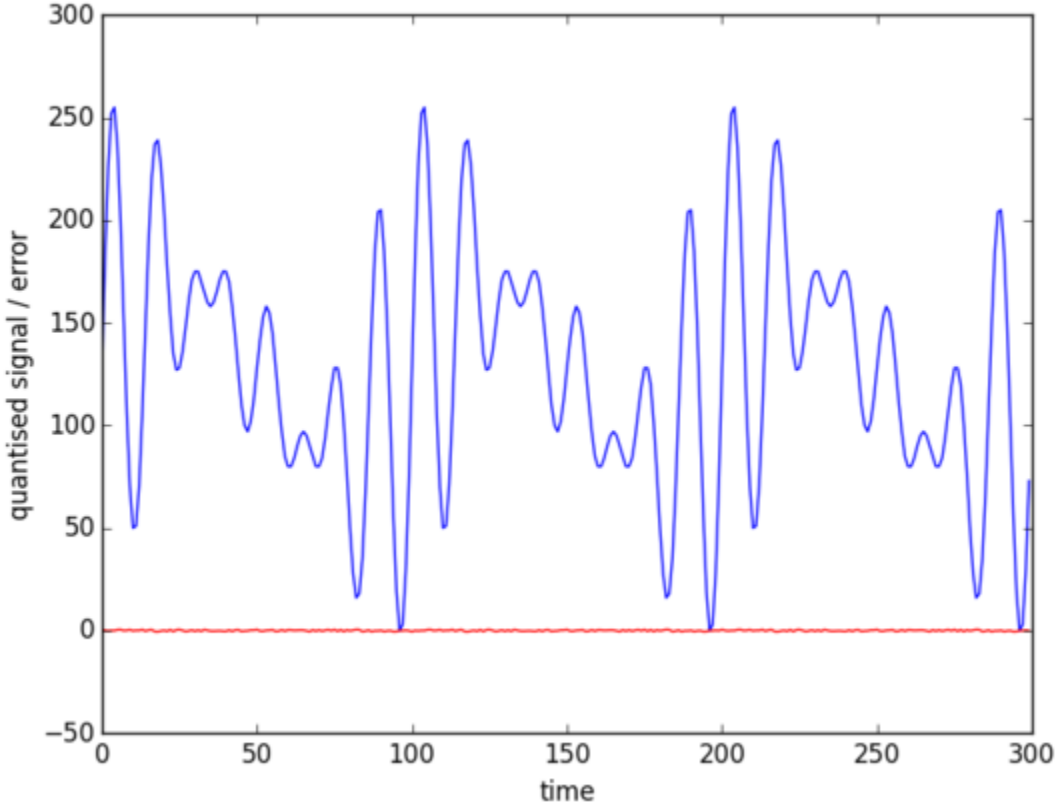
- Signals are floats
- FIR consists of integer operation blocks
- Quantization is required – will it work?



Simulation in python

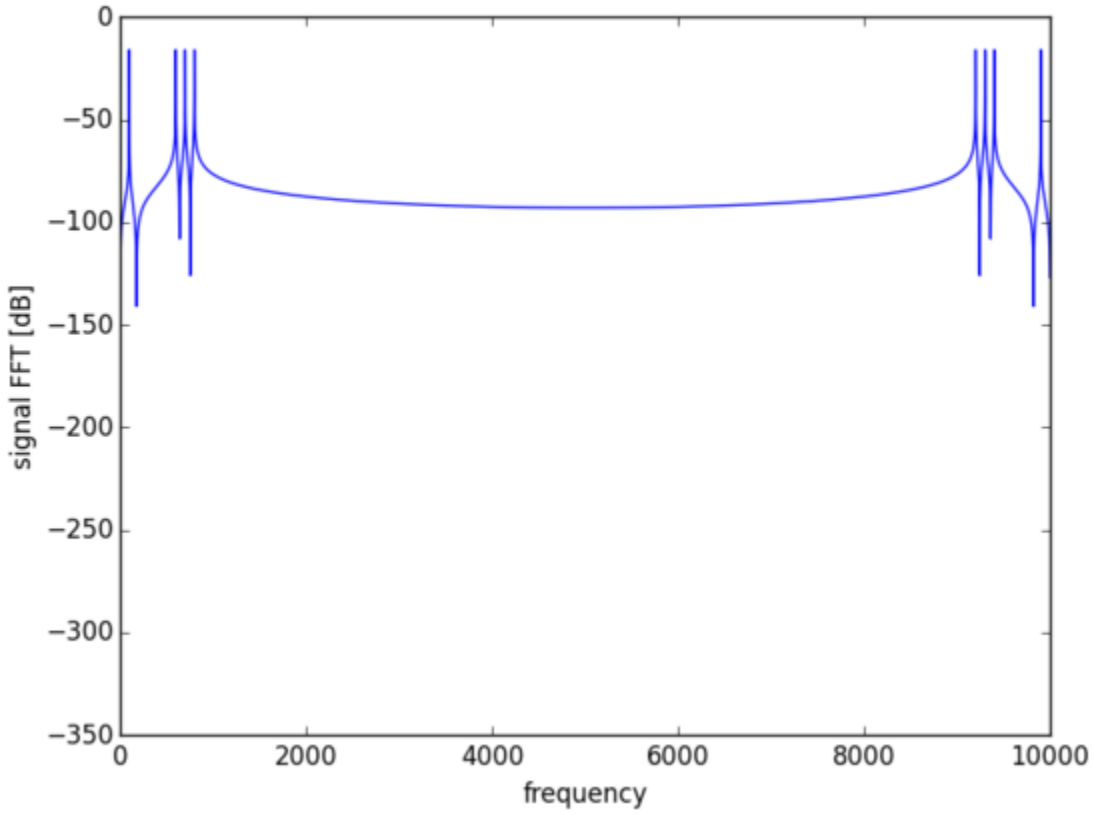


Original signal consisting of 4 harmonics.

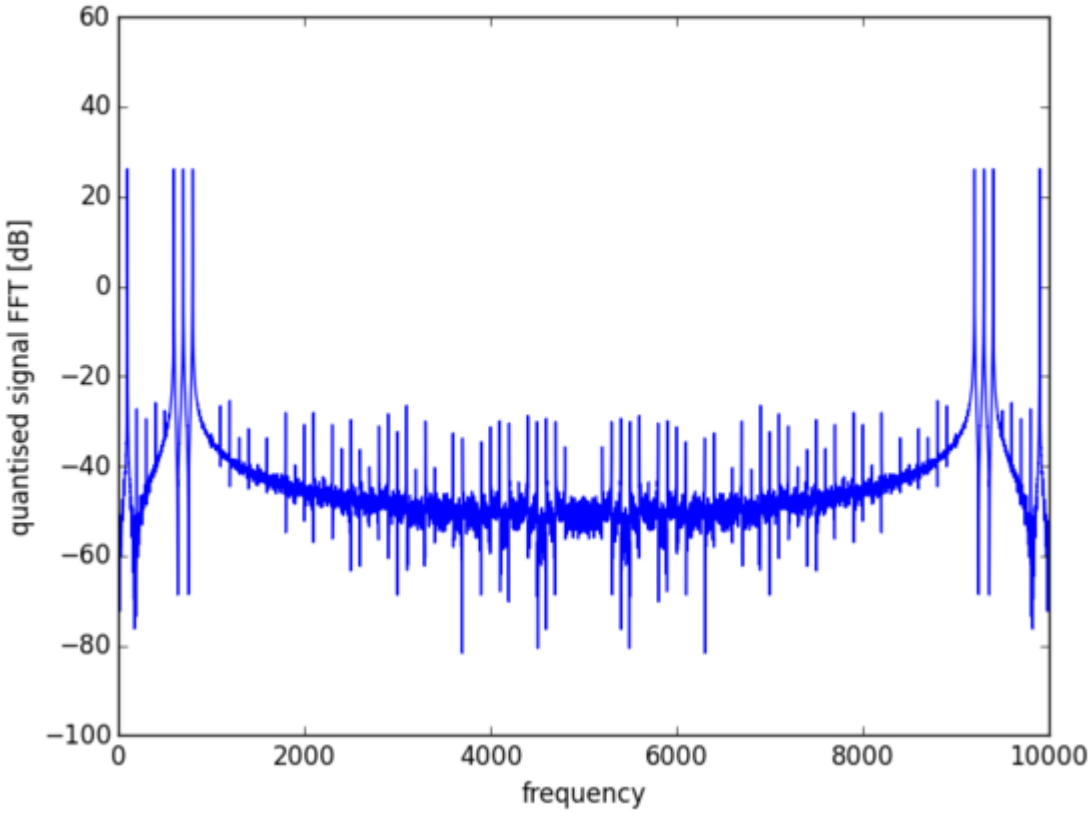


Quantized signal and quantization error.

Simulation in python



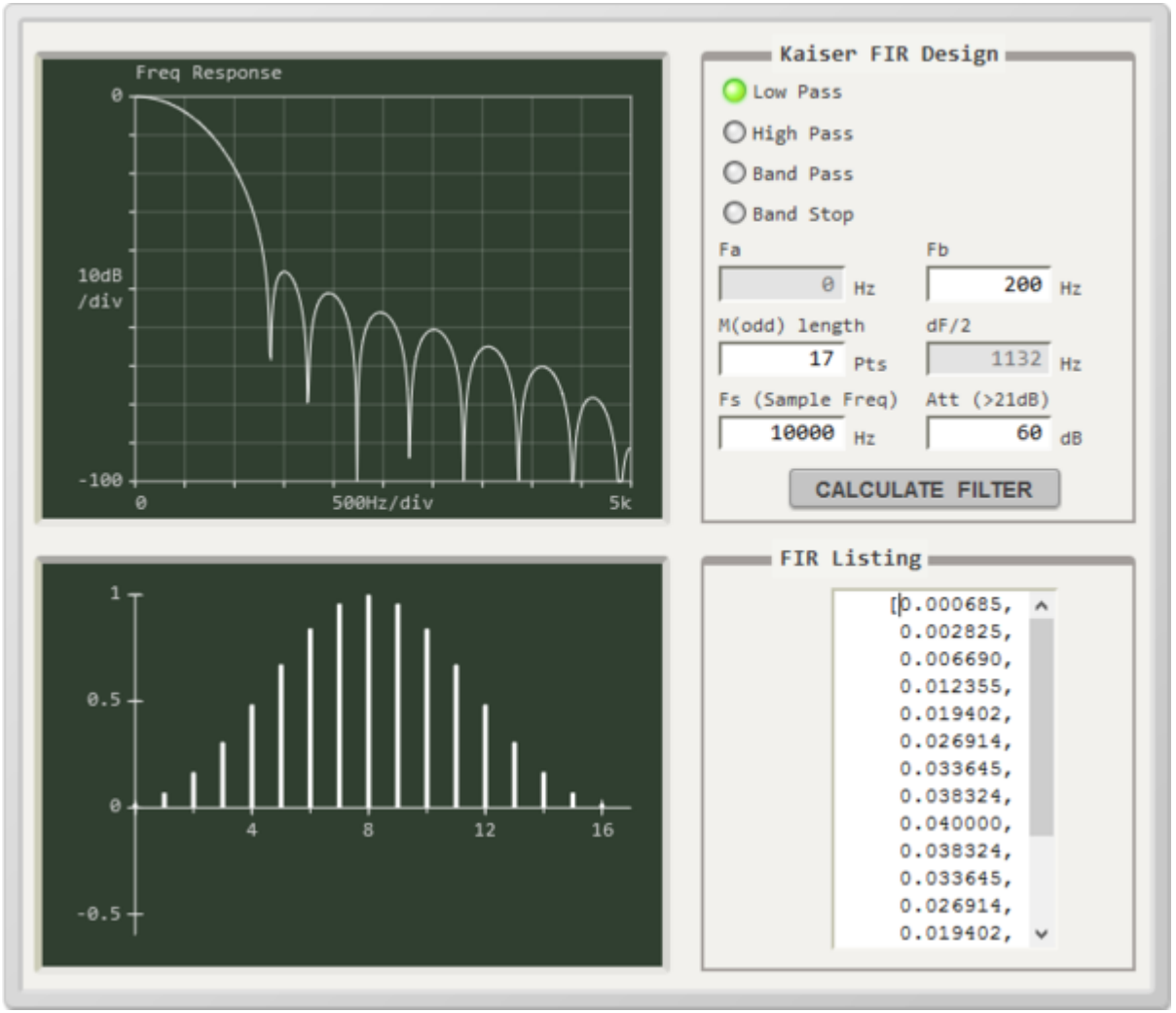
Original signal frequency distribution.



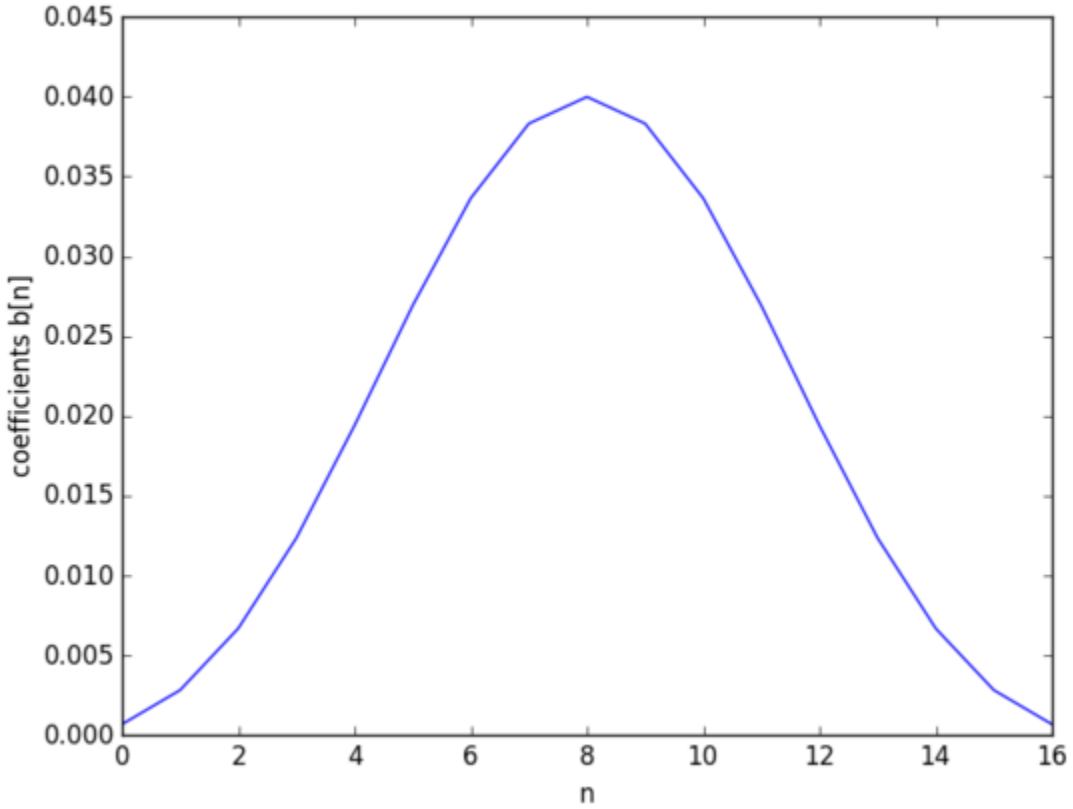
Quantized signal frequency distribution.

Simulation in python

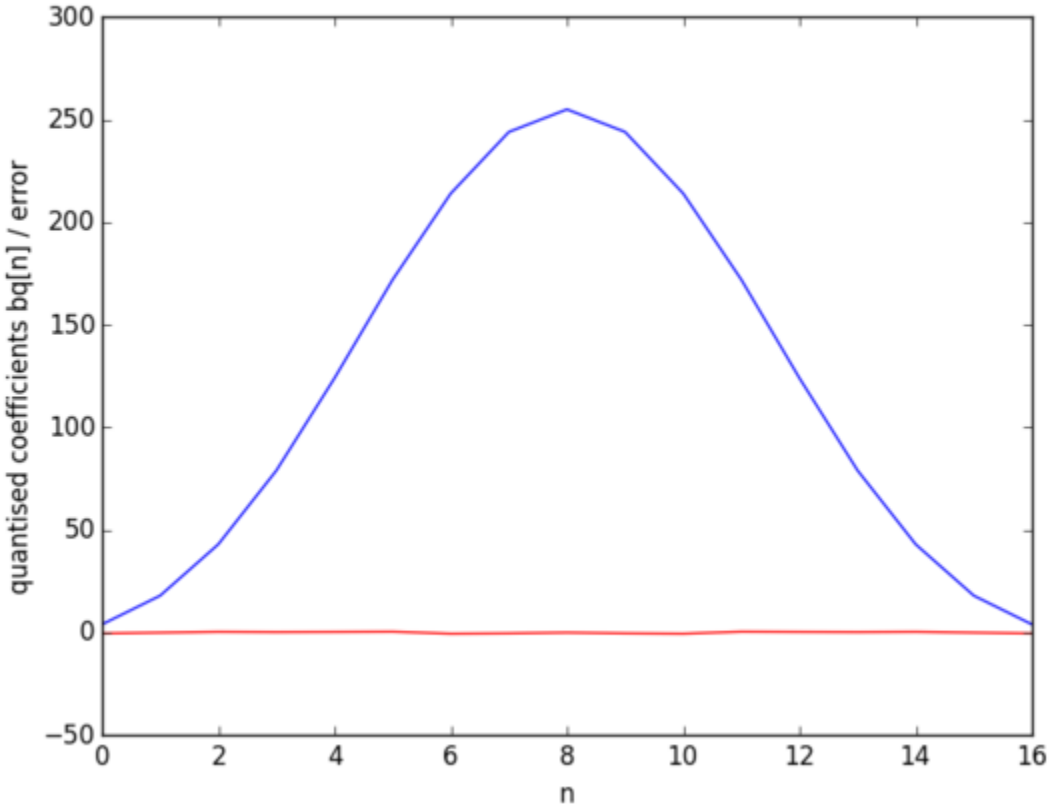
Filter generated coefficients based on desired frequency response [4].



Simulation in python

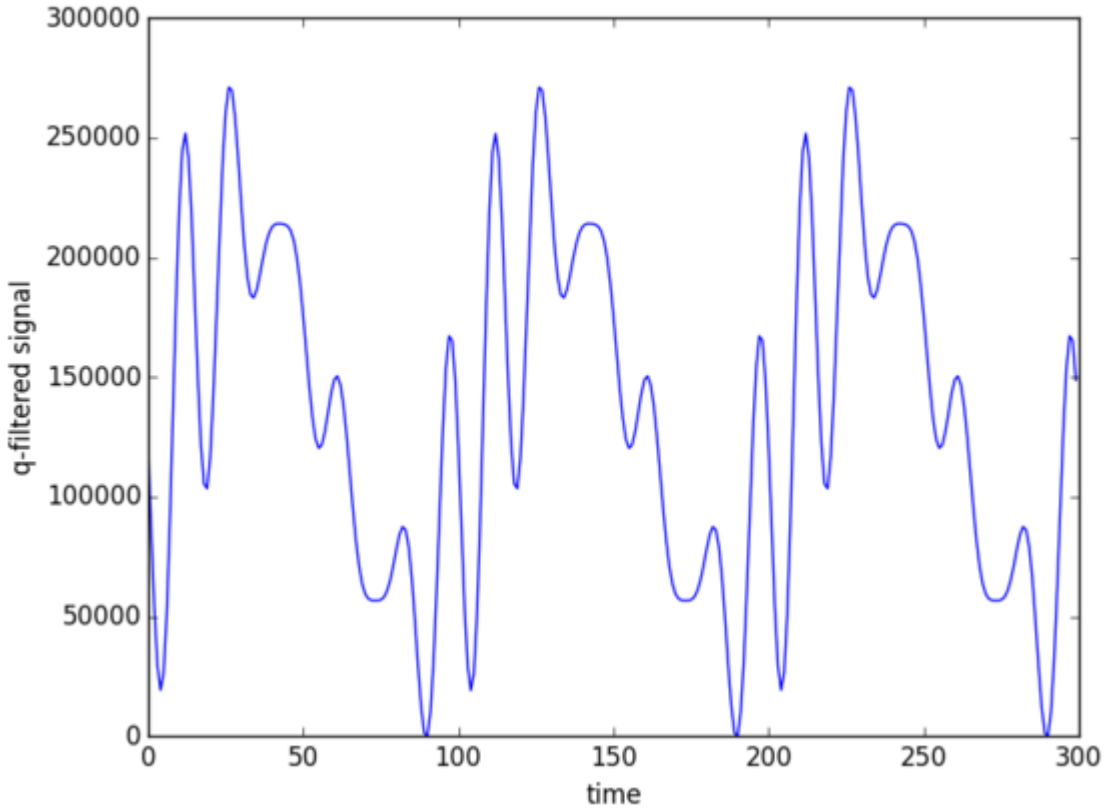


Coefficients of N=17 FIR filter.



Quantized coefficients and quantization error.

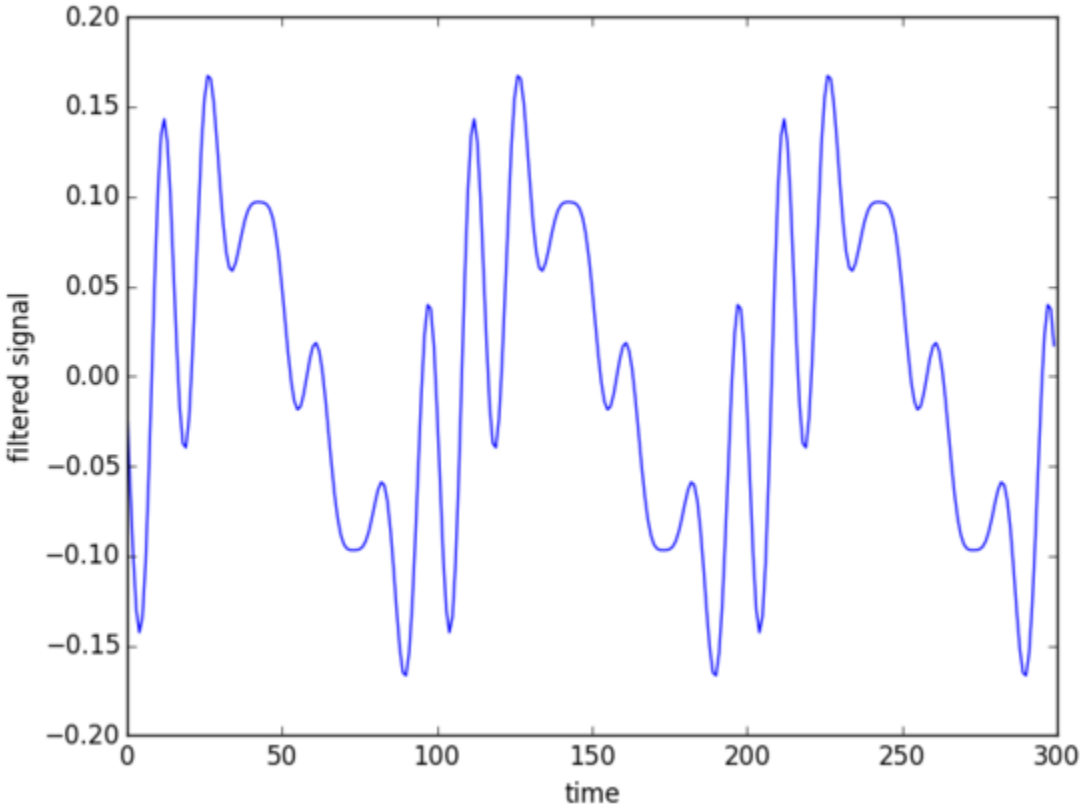
Simulation in python



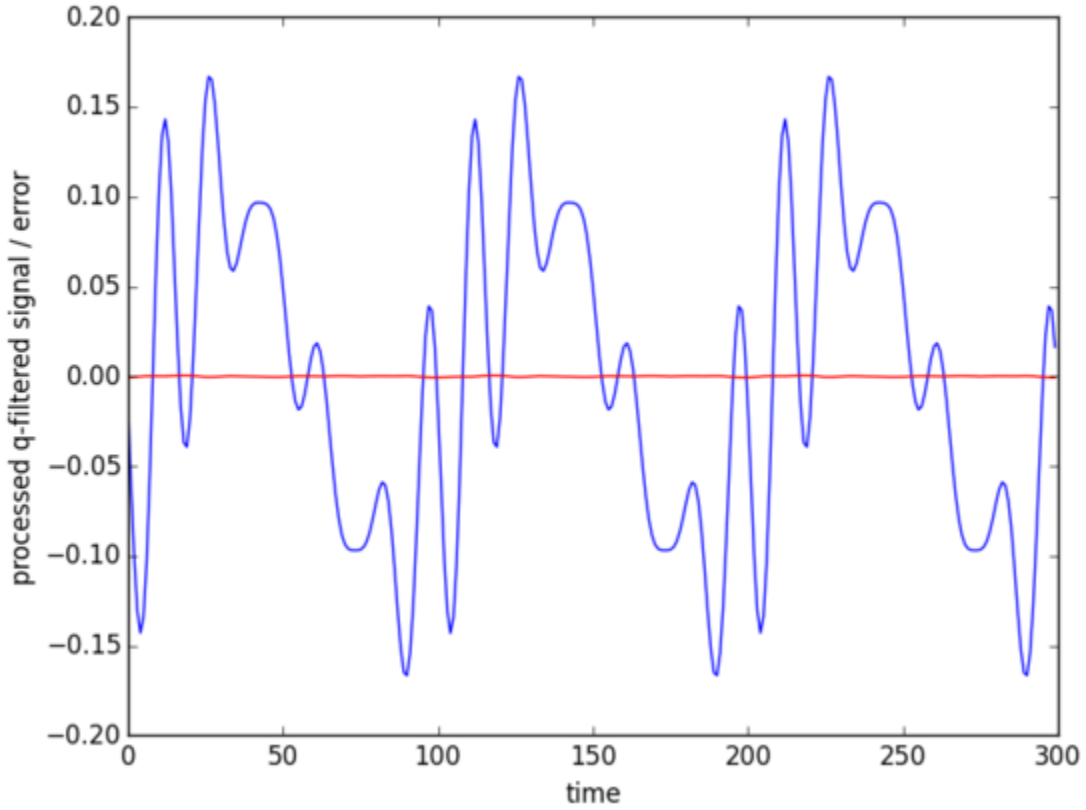
Pre-processed quantized filter output.

Range = 0 to 271065
19-bit value !!!

Simulation in python

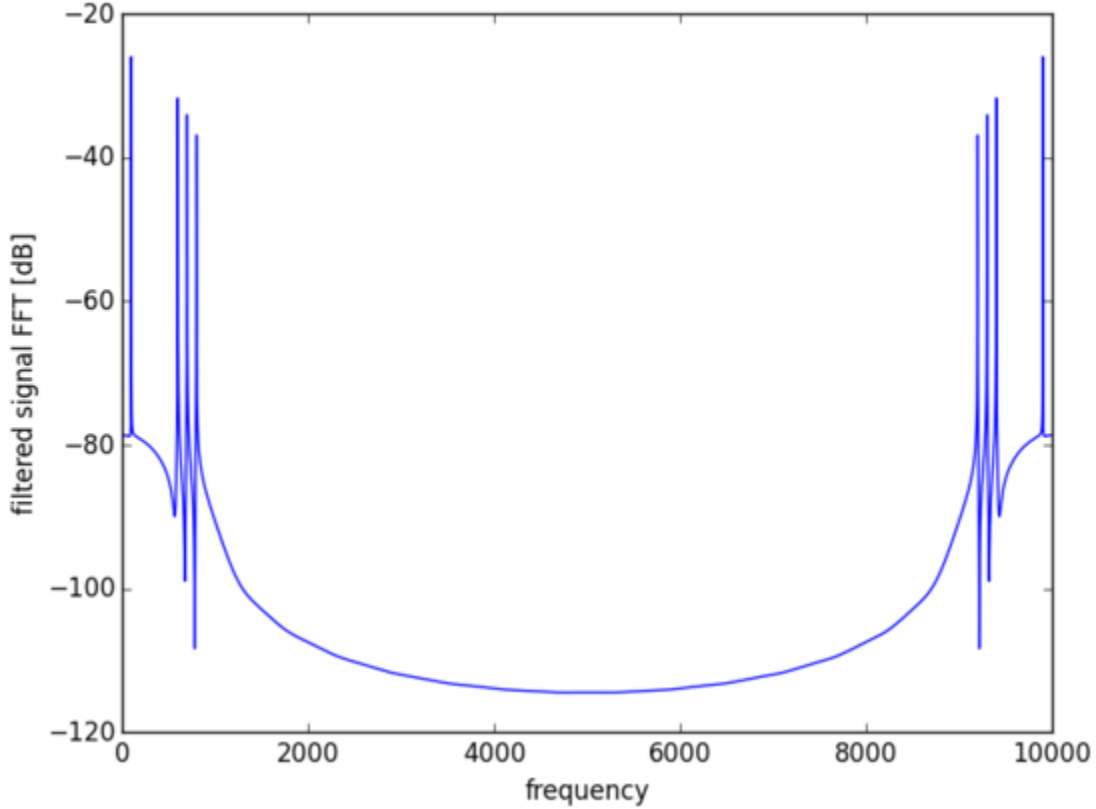


Filtered signal using float operations.

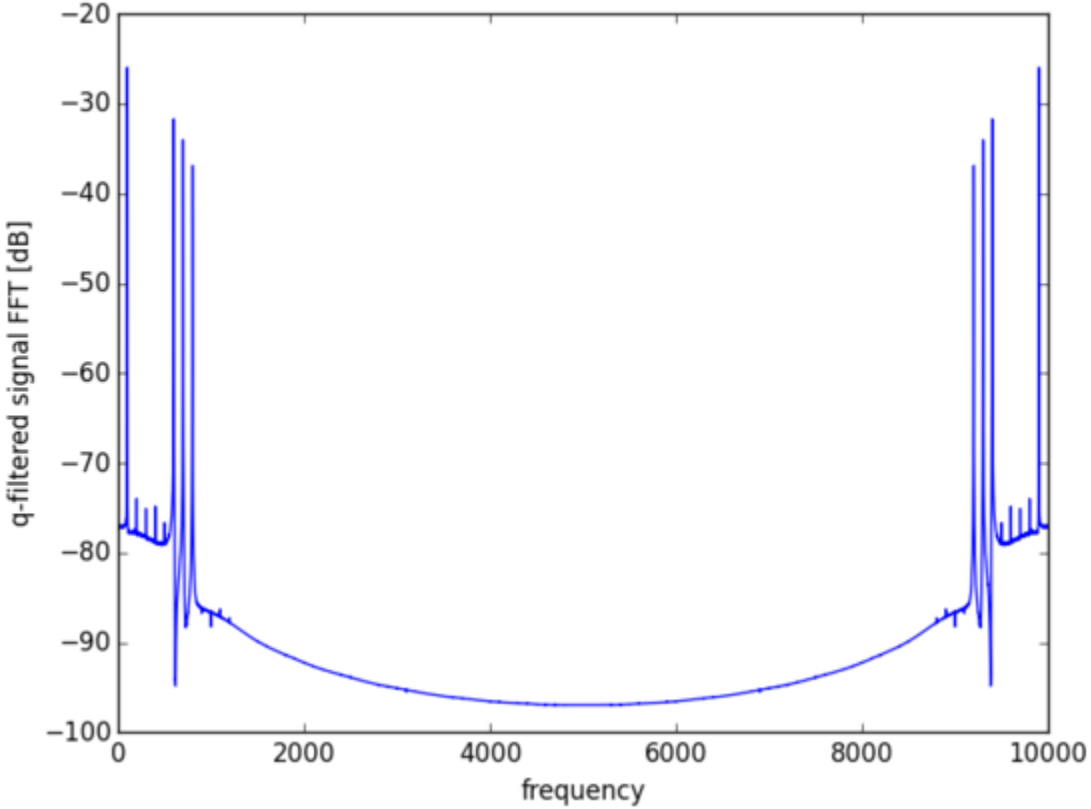


Processed quantized filter output and total error.

Simulation in python

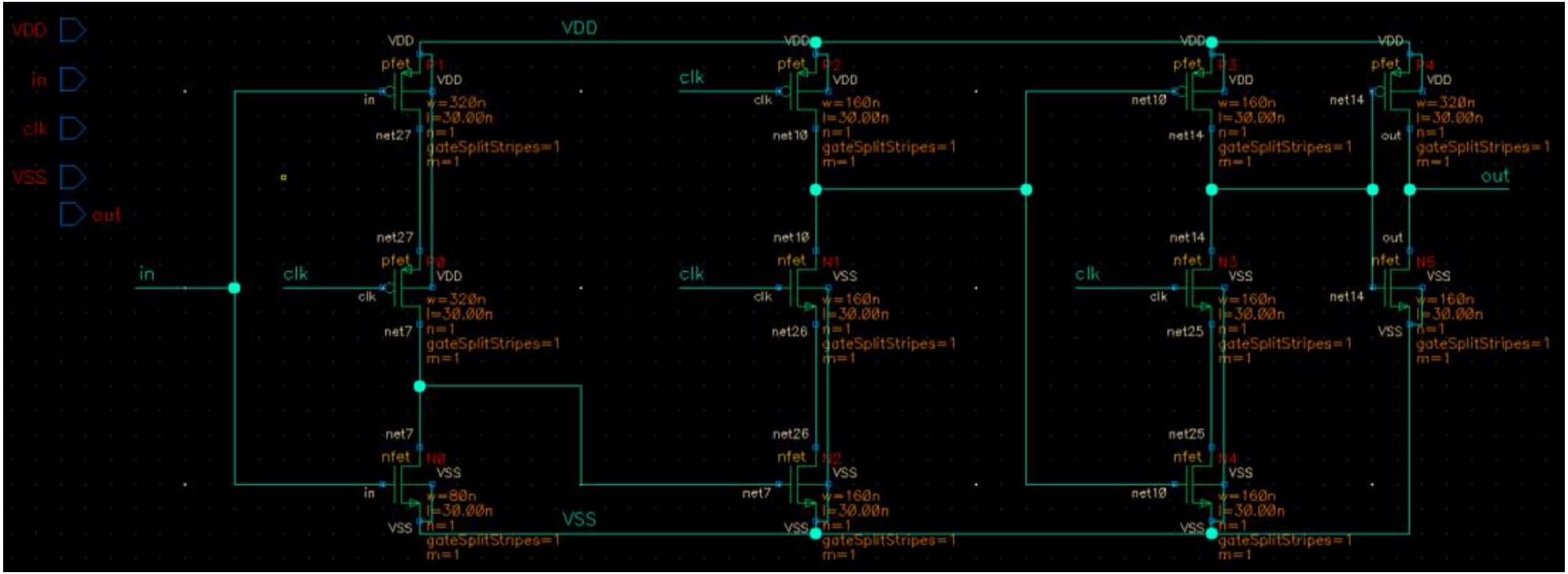


FFT of filtered signal using float operations.



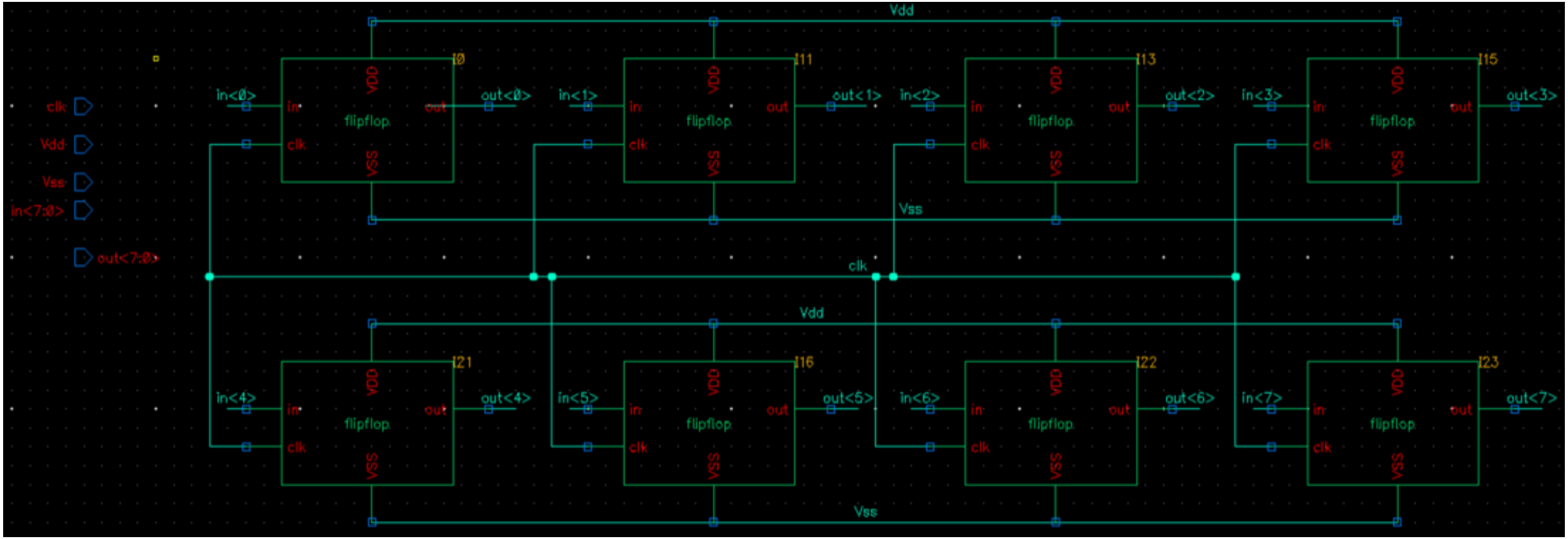
FFT of quantized filtered signal.

True Single Phase Clocked flipflop design



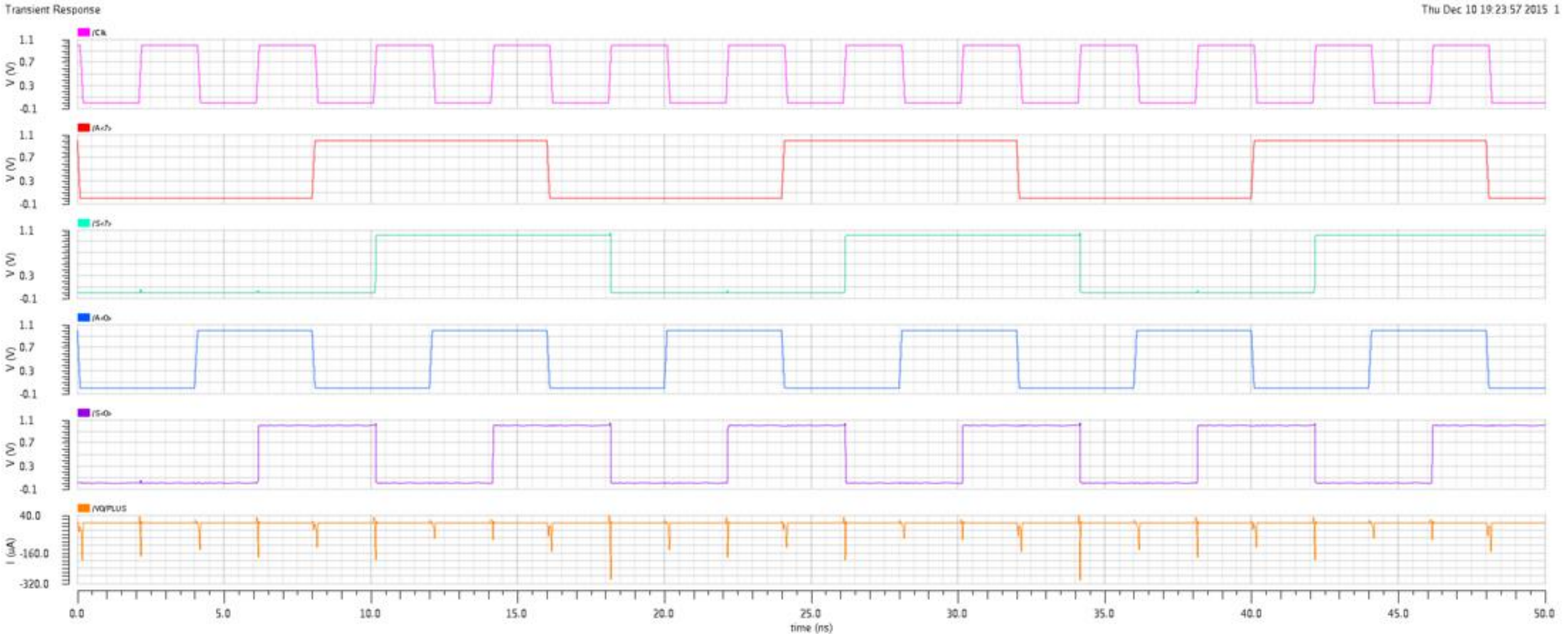
Schematic diagram of a TCSP flipflop.

True Single Phase Clocked flipflop design



Schematic diagram of the 8-bit flipflop.

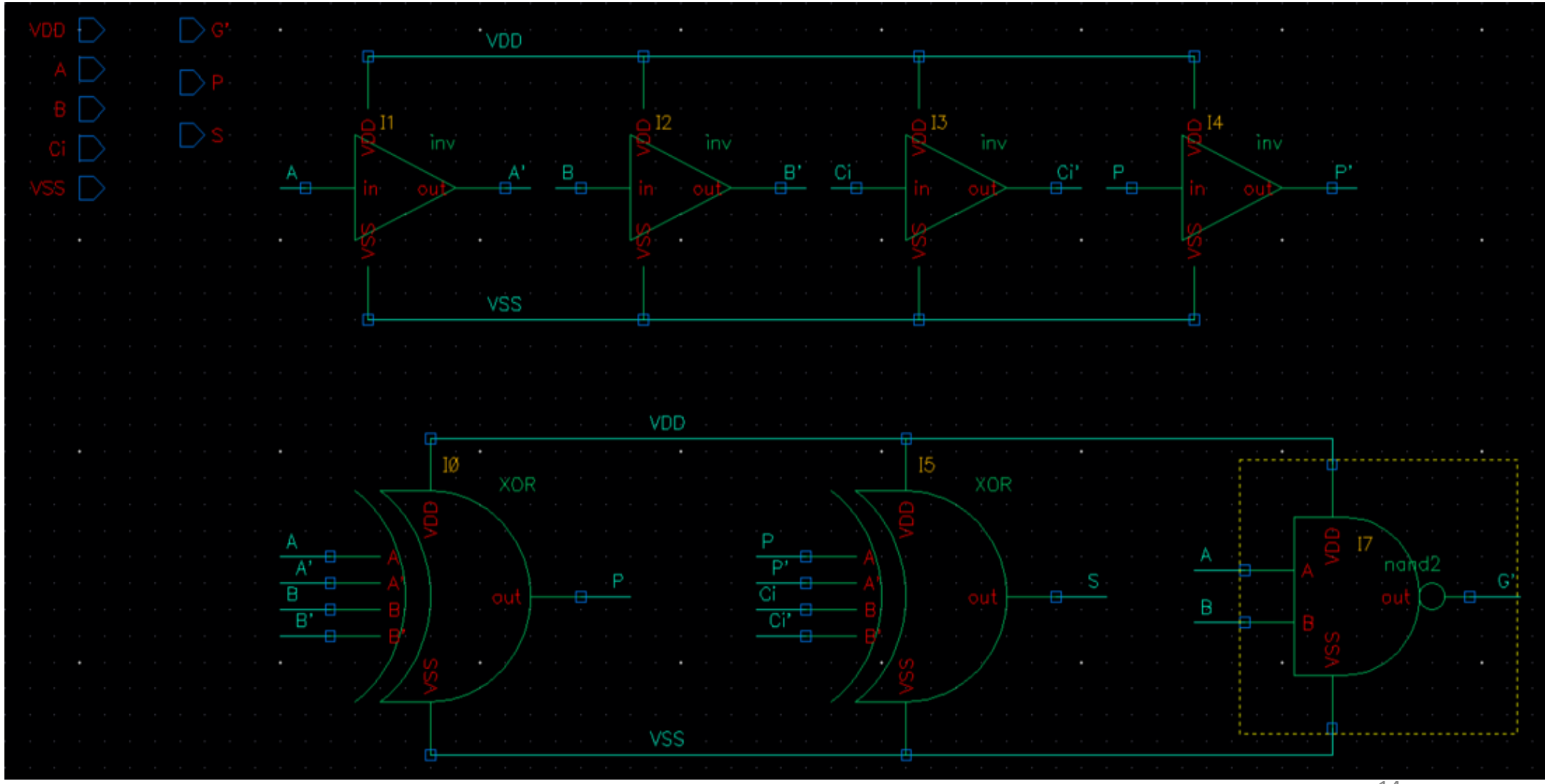
TSPC flipflop simulation



TSPC flipflop 8-bit block delay element simulation.

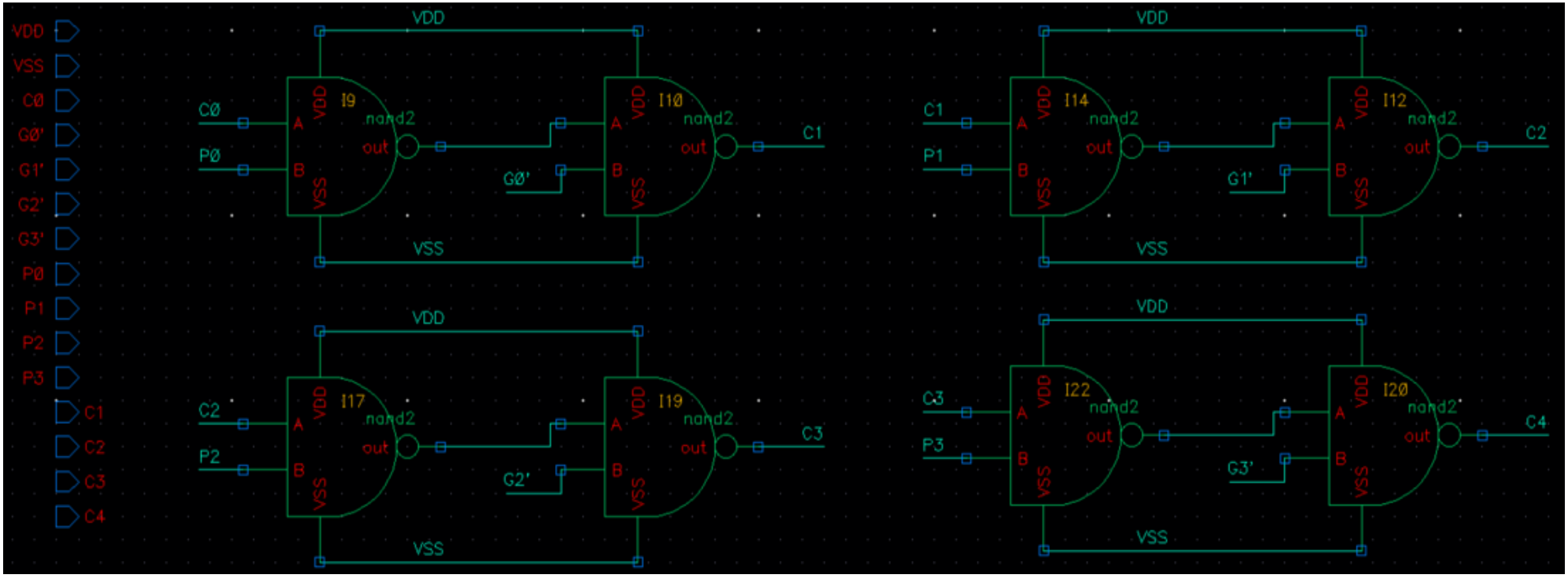
Carry Look Ahead (CLA) Adder

- Propagate
- Generate
- Sum



CLA Partial Full Adder component schematics.

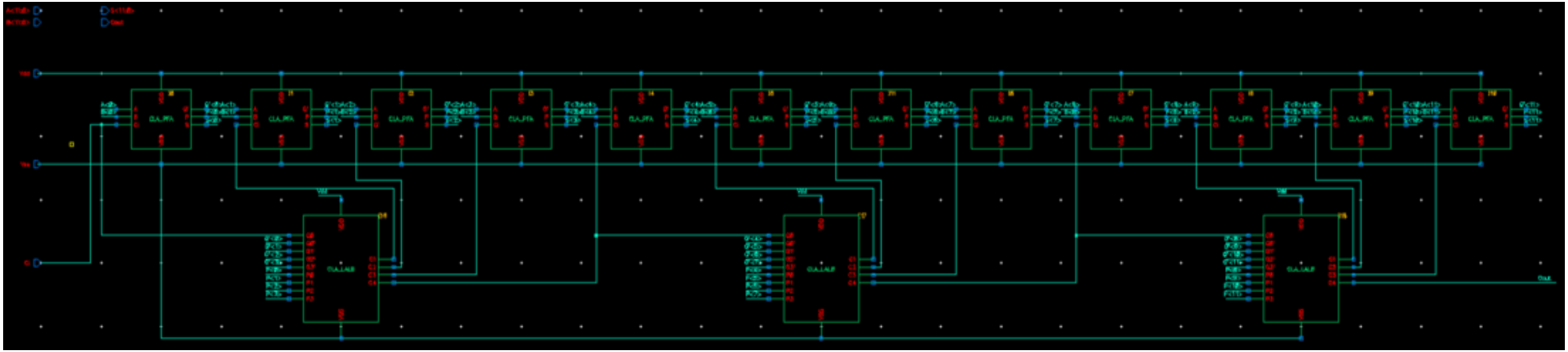
Carry Look Ahead (CLA) Adder



Look Ahead Logic Block Schematics.

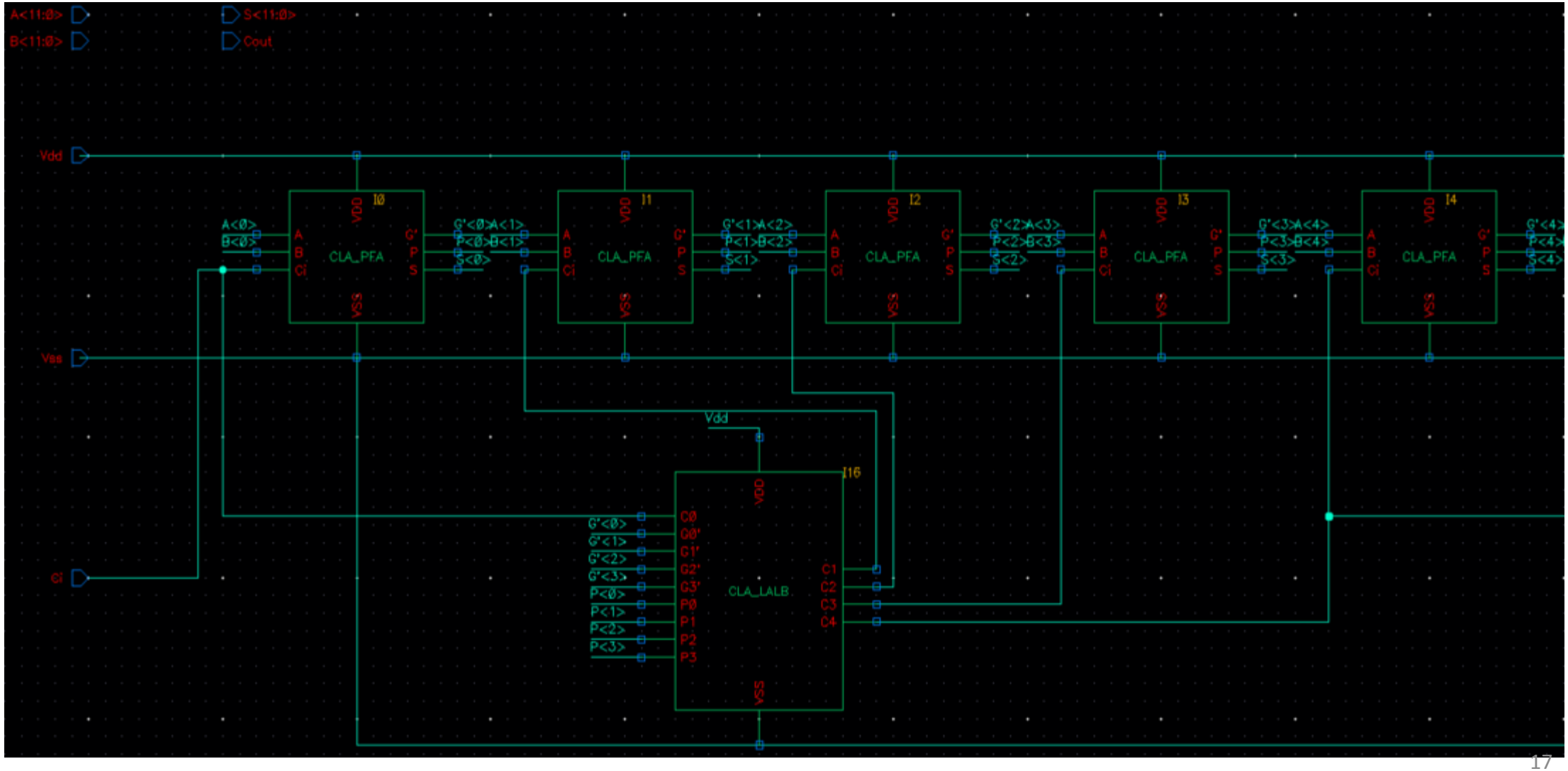
- Uses P, G and S to compute the Carry bits

Carry Look Ahead (CLA) Adder



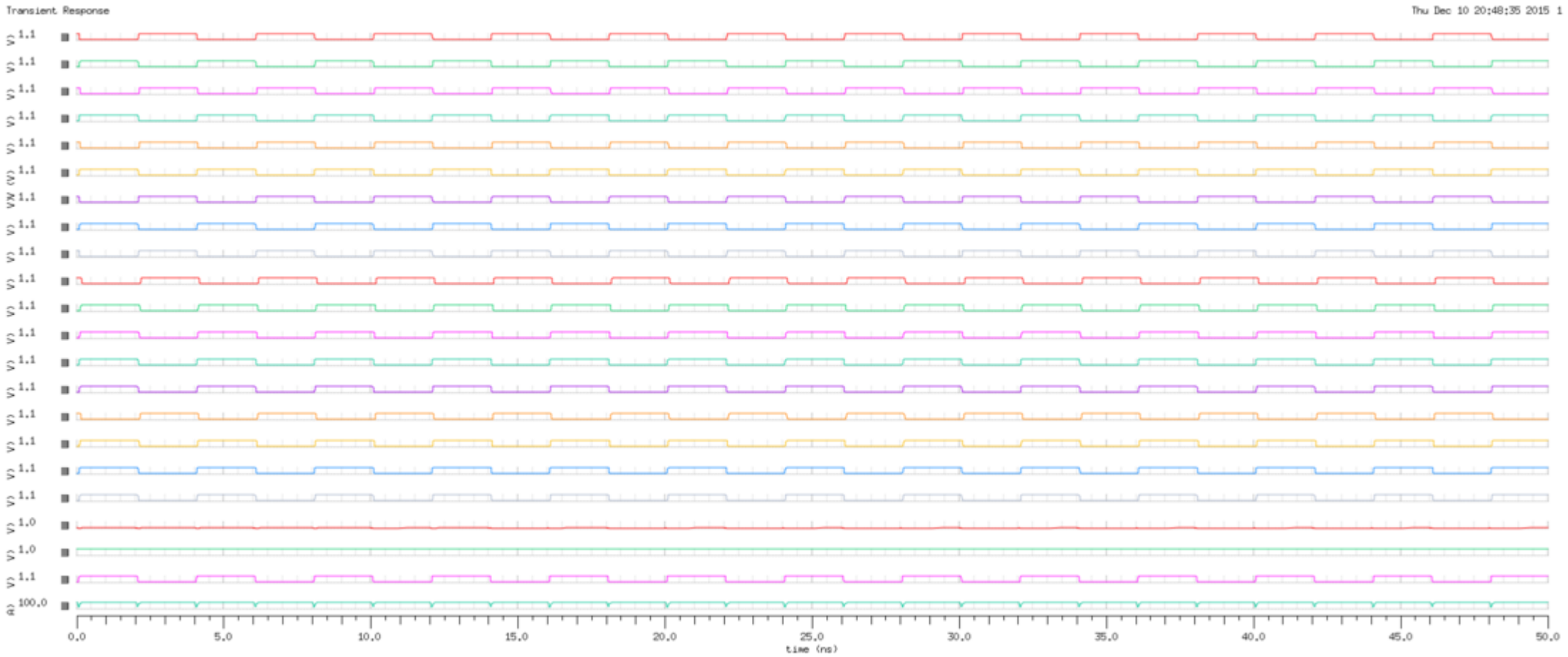
12-bit CLA adder full schematics.

Carry Look Ahead (CLA) Adder



12-bit CLA adder full schematics in more detail.

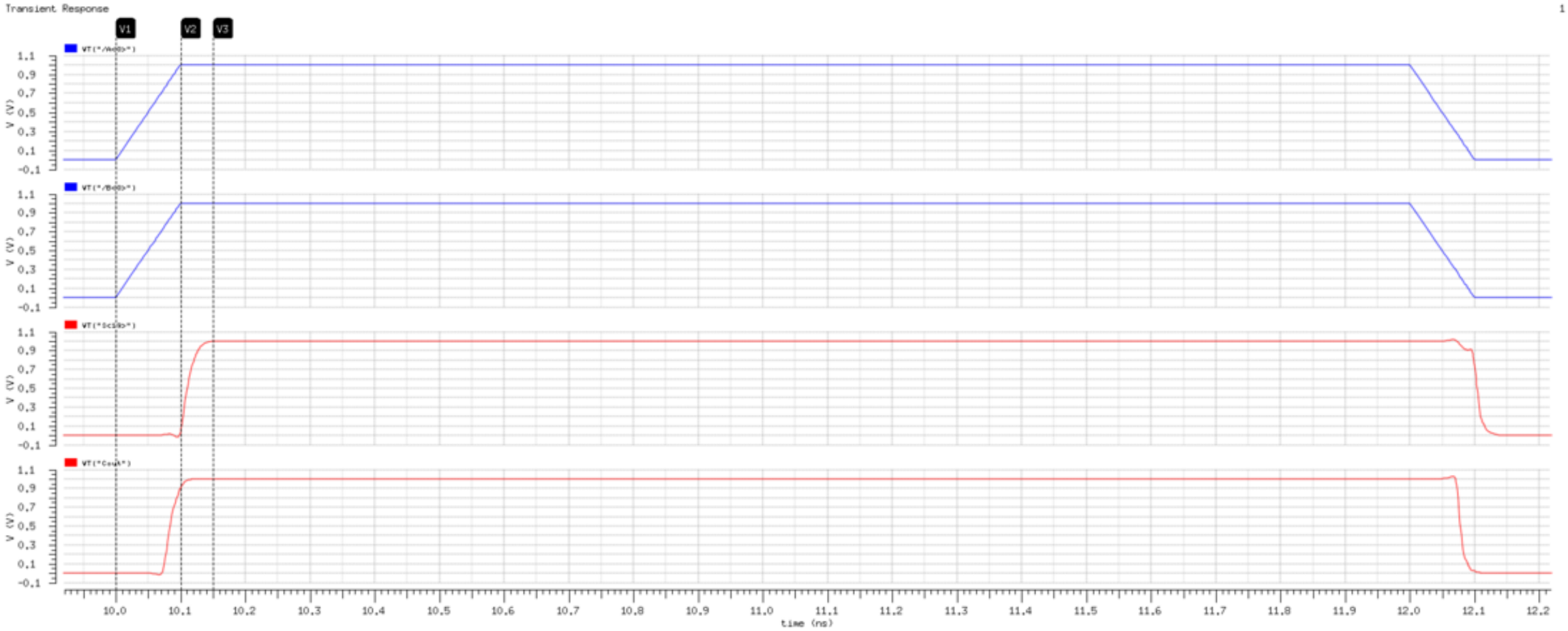
Carry Look Ahead (CLA) Adder Simulation



Carry Look Ahead adder simulation.

We tested the adder with several inputs and the results were correct. Critical test: adding all-1 signals. ✓

Carry Look Ahead (CLA) Adder Simulation



Carry Look Ahead adder delay.

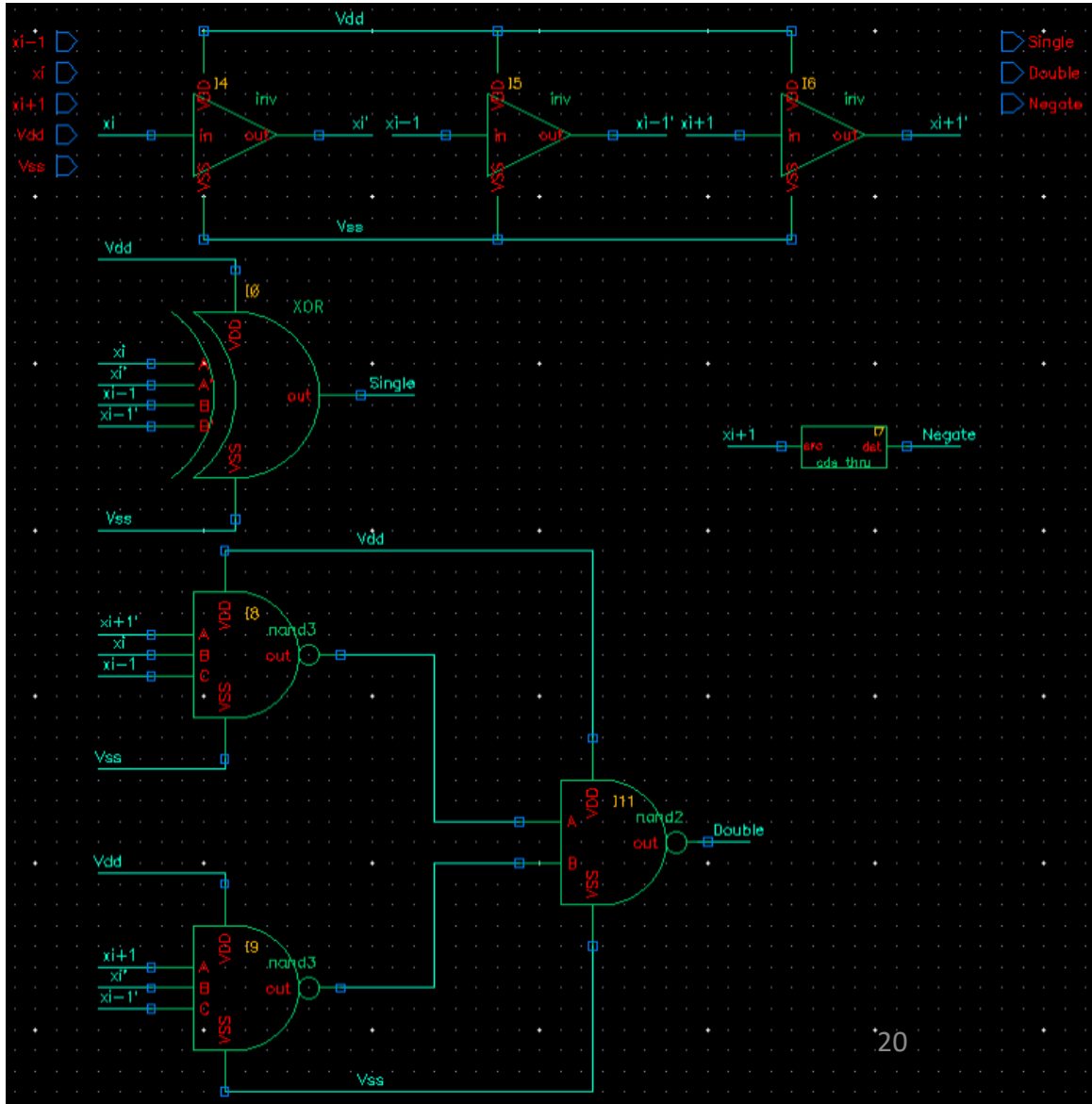
The measured critical delay is $t_{HL} \approx t_{LH} = 0.15ns$.

8x8 radix-4 Booth Multiplier

Grouping	Partial Product	Comments
0	0*M	string of zeros
1	1*M	a single 1
10	1*M	a single 1
11	2*M	end of ones
100	-2*M	beginning of ones
101	-1*M	beginning of ones
110	-1*M	beginning of ones
111	0*M	string of ones

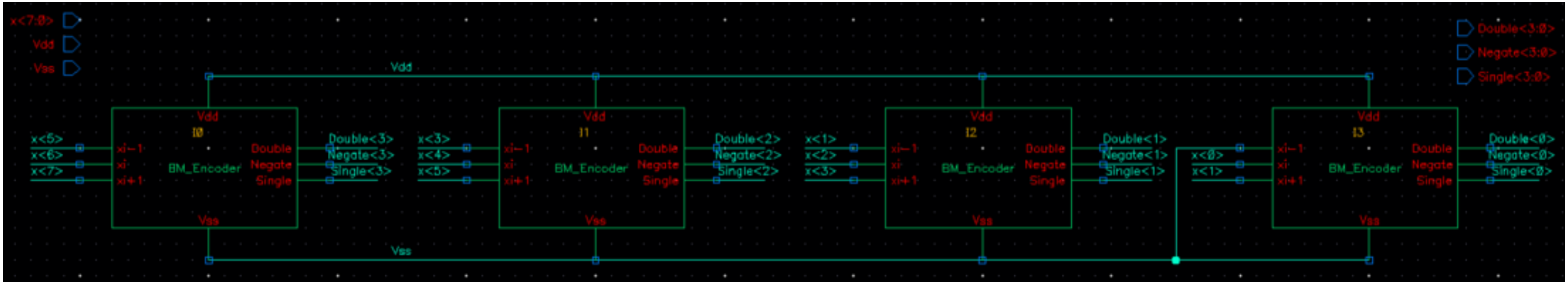
Computes:

- Single
- Double
- Negate



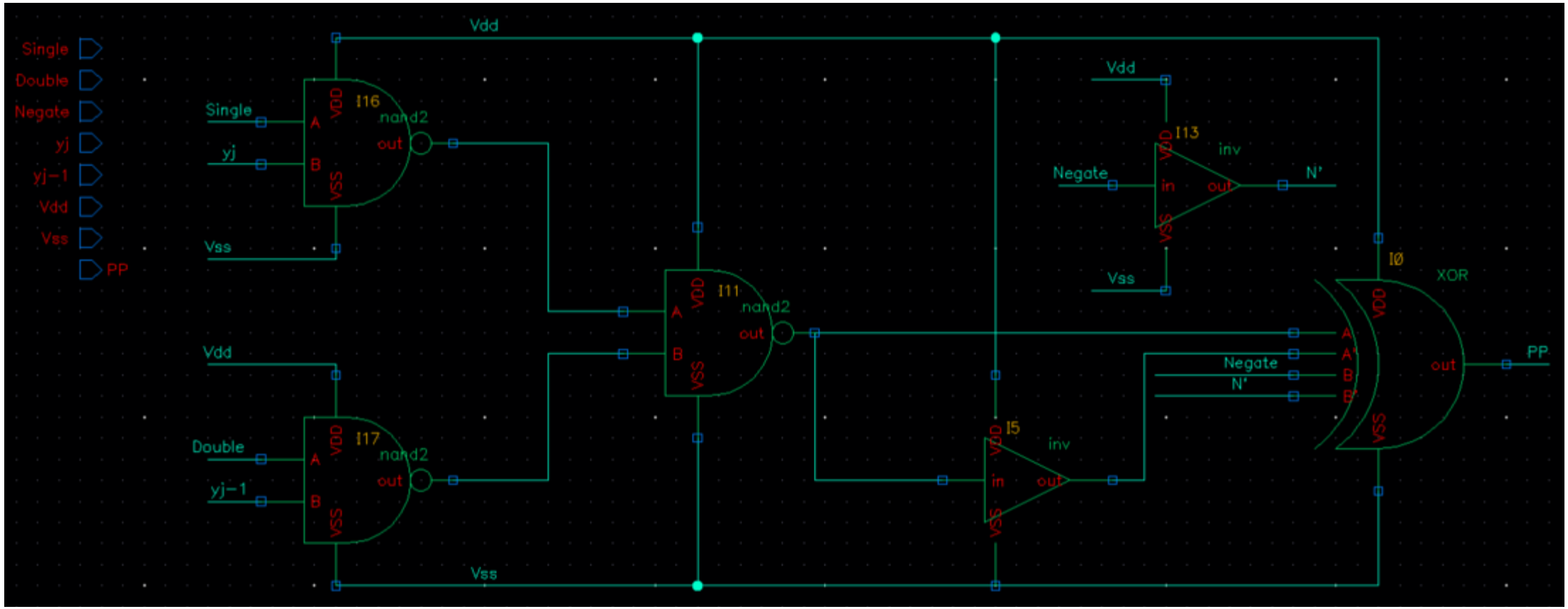
Encoder Schematics.

8x8 radix-4 Booth Multiplier



Full Encoder Schematics for 8-bit multiplier.

8x8 radix-4 Booth Multiplier

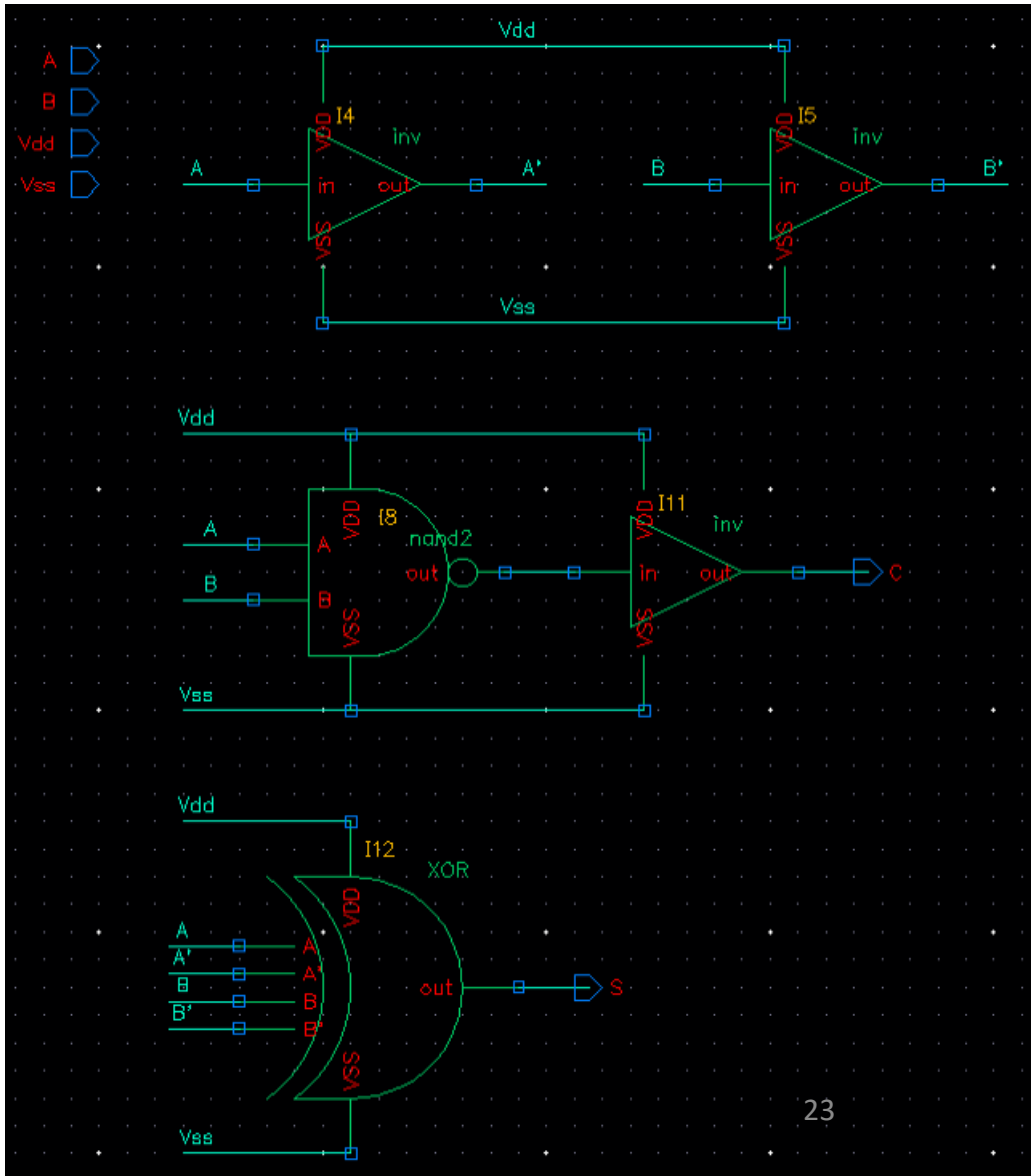


Decoder Schematics.

- Uses the Single, Double and Negate to compute partial products.

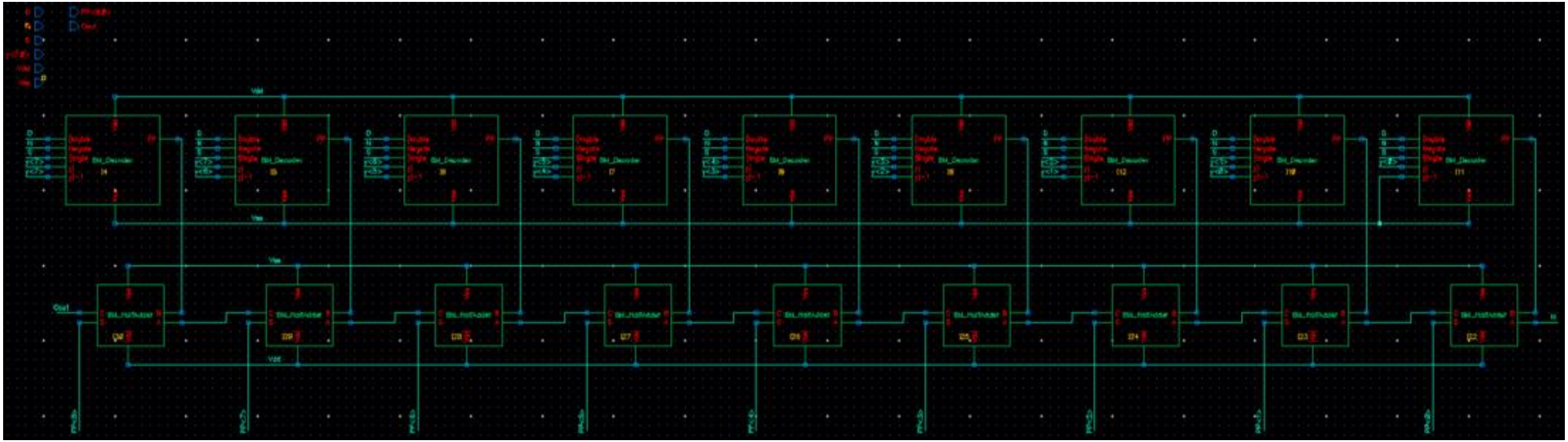
8x8 radix-4 Booth Multiplier

- Half adder necessary to implement two's complement negation.



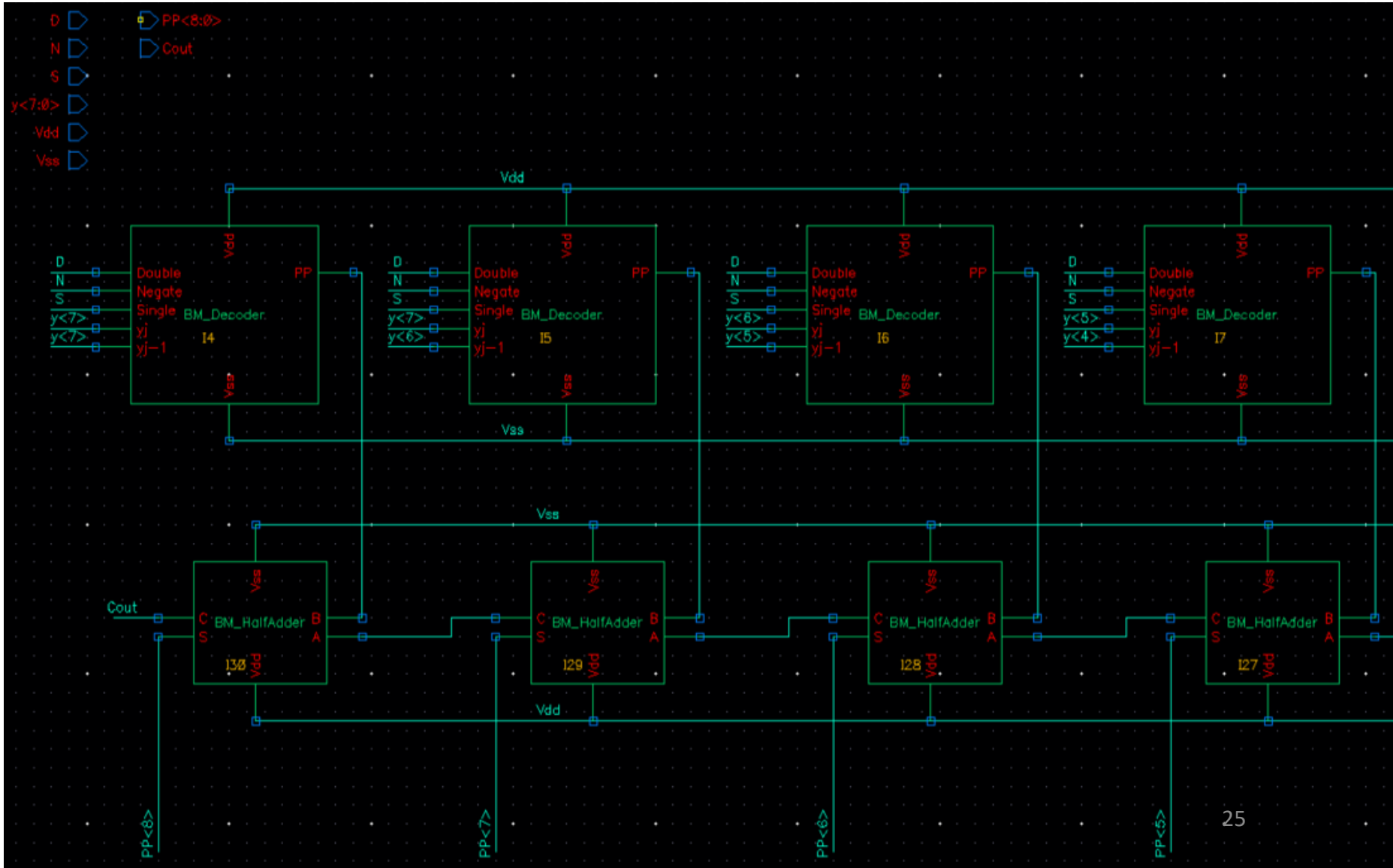
Half Adder Schematics.

8x8 radix-4 Booth Multiplier



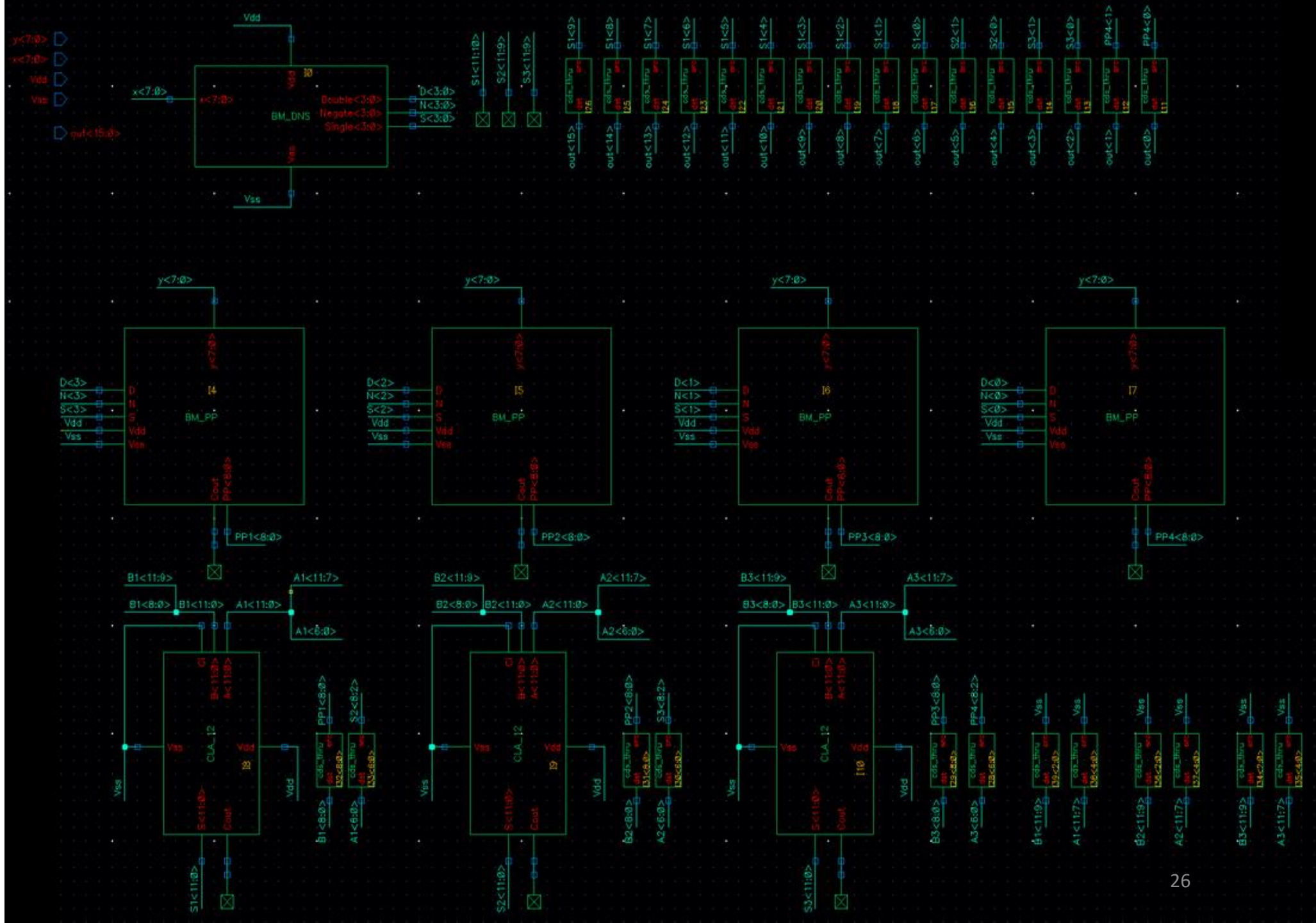
Full Decoder Schematics.

8x8 radix-4 Booth Multiplier

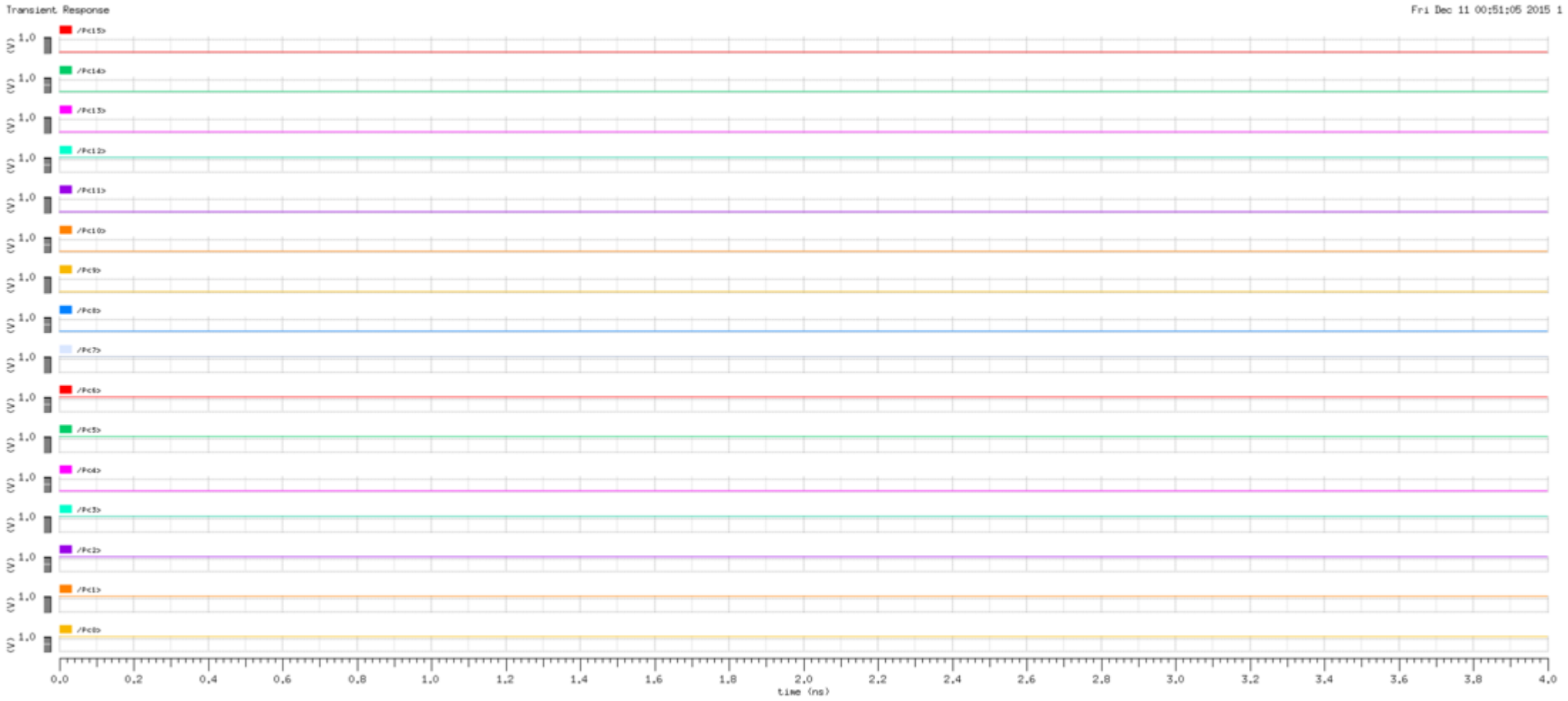


Full Decoder Schematics in detail.

Full Multiplier Schematics.

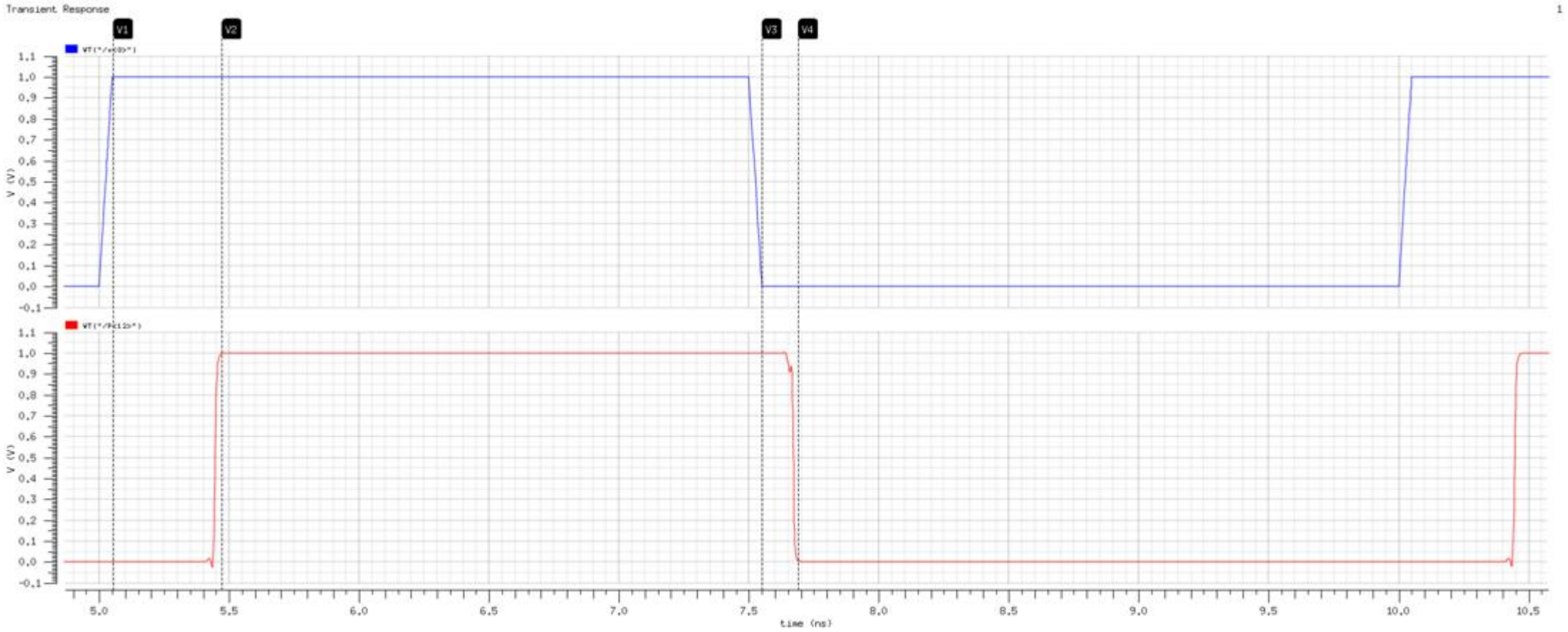


8x8 radix-4 Booth Multiplier simulation



Test simulation 110011x1010101=1000011101111.

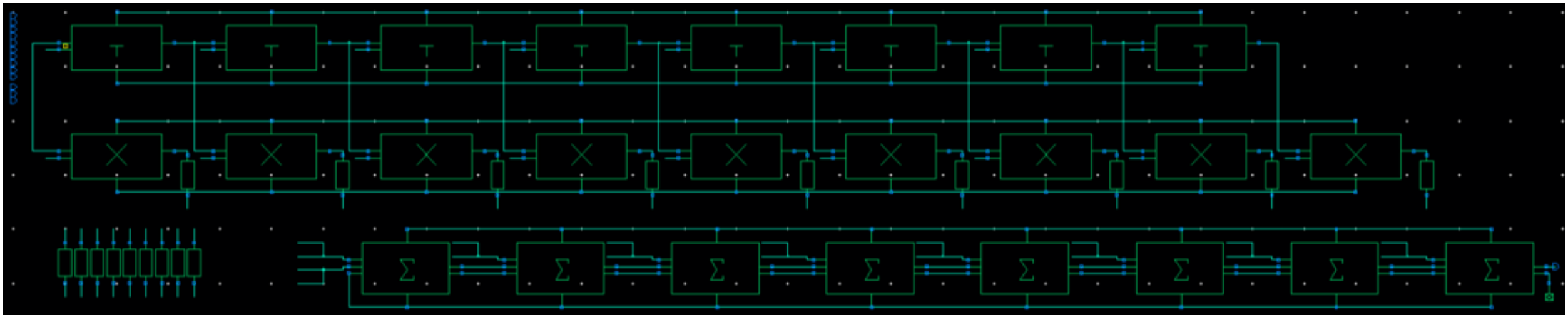
8x8 radix-4 Booth Multiplier simulation



Multiplier Delay

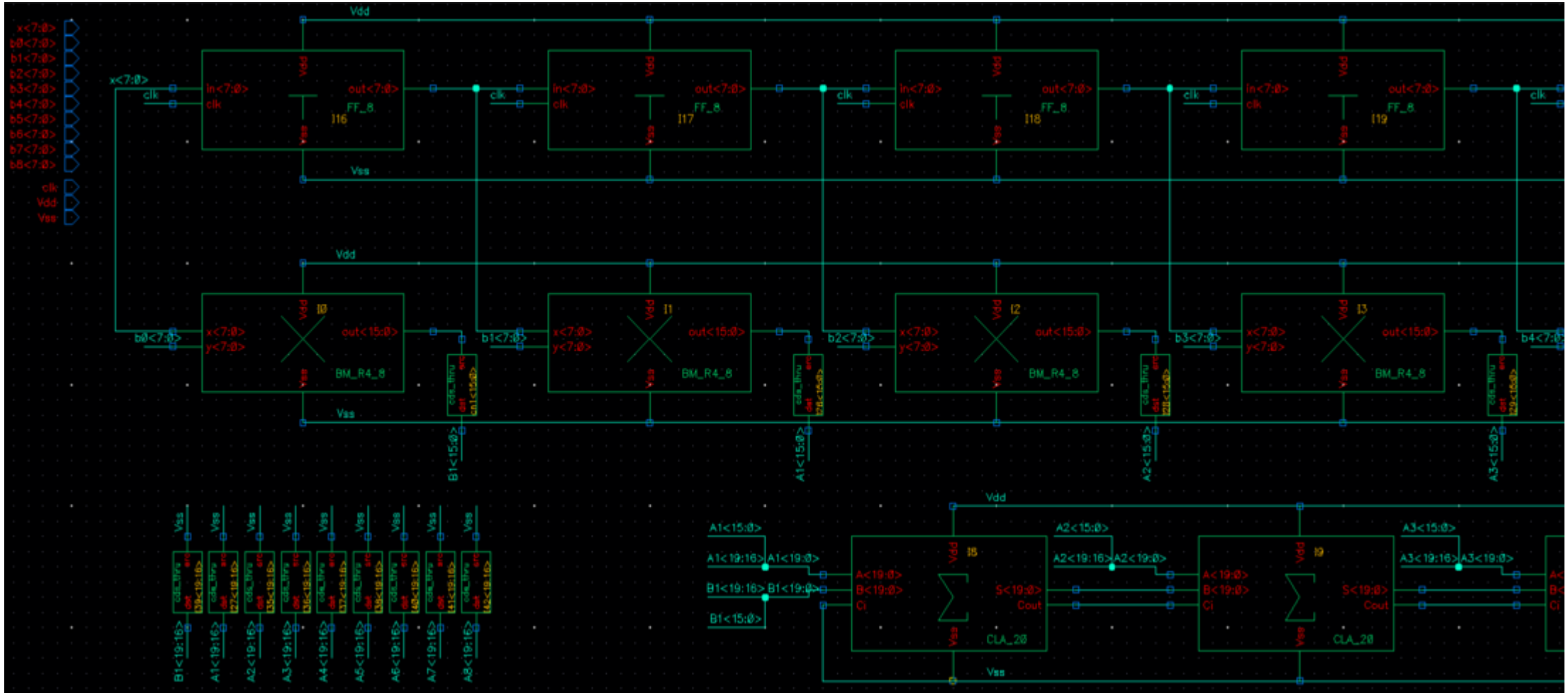
- The critical delay measured is $t_{LH} = 0.42\ ns$, $t_{HL} = 0.14\ ns$.

Finite Impulse Response Filter



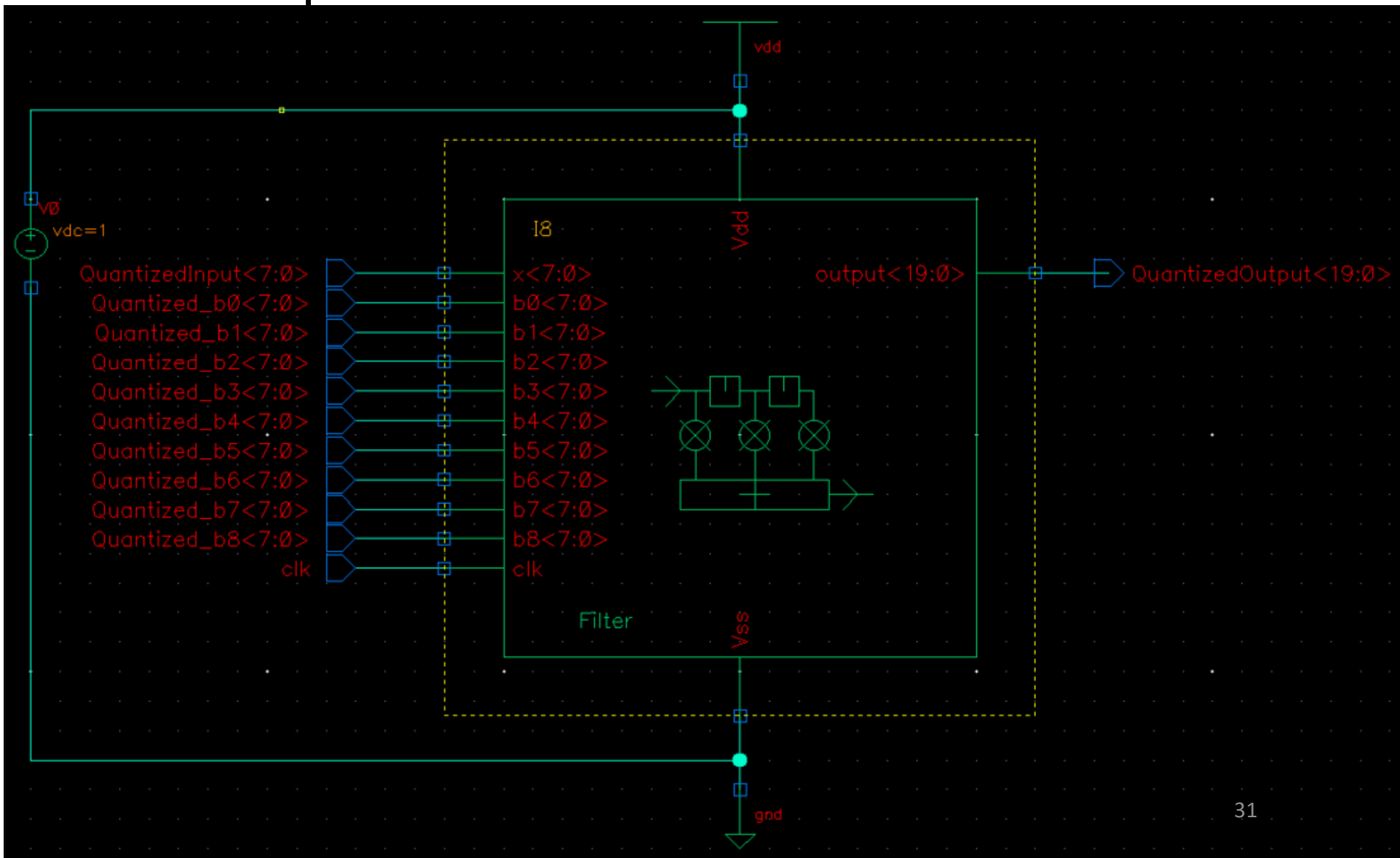
FIR schematics overview

Finite Impulse Response Filter



FIR schematics in more detail

Finite Impulse Response Filter



FIR Filter Testbench

Results and Conclusion

Gate	# transistors
Flipflop	11
8-bit flipflip	88
CLA PFA	32
CLA LALB	64
12-bit CLA	576
20-bit CLA	960
Encoder	38
Decoder	36
Half Adder	22
8-bit Multiplier	2858
FIR (total)	31034

Block	Leakage 0	Leakage 1	Total Dynamic power
8-bit flipflop	20 nW	15.9 nW	2.1 µW
20-bit CLA adder	26.2 nW	30.8 nW	33.4 µW
8-bit BM	102.2 nW	117.8 nW	46 µW

- VLSI is fun! (and hard work!)
- Achieved successful operation for the flipflops, carry look-ahead adder and booth encoding multiplier
- Optimized sizing for improved delay times and reduced glitches

- Perform Corners simulations and Monte Carlo Process Variation

References

- [1] Technology CMOS28FDSOI 28 nm SOI 3D
- [2] Latches and Flip-Flops by Dr. Paul D. Franzon, NCSU
- [3] CMOS Binary Full Adder - A Survey of Possible Implementations by E. Turgay, A. Daniels, M. Bacelieri, W. Berry, UKY
- [4] arc.id.au FIR Filter Design
- [5] Design of an 8x8 Modified Booth Multiplier by Robbie D'Angelo and Scott Smith
- [6] Digital Computer Arithmetic by Israel Koren, University of Massachusetts